

Claims

What is claimed is:

1. An integrated circuit, comprising:
2 a sensor operable to detect performance variations of an individual circuit in said
3 integrated circuit, said performance variation being related to aging of said
4 integrated circuit; and

5 a compensation circuit operable to change the operating characteristics of said
6 individual circuit to compensate for said performance variation in
7 accordance with an aging-versus time performance curve.

1 2. The integrated circuit of claim 1, wherein the individual circuit comprises a phase-
locked loop.

1 3. The integrated circuit of claim 2, wherein the compensation circuit comprises a
2 charge pump having multiple legs that can be selectively enabled to change the performance
3 characteristics of said phase-locked loop.

1 4. The integrated circuit of claim 2, wherein compensation circuit comprises a power
2 supply controlled by digital control words to selectively change the operating characteristics
3 of said phase-locked loop.

1 5. The integrated circuit of claim 2, comprising a ring oscillator operable to
2 approximate the effects of NBTI and to generate a compensation signal corresponding
3 thereto.

1 6. The integrated circuit of claim 5, wherein said compensation signal is used to
2 generate digital control words to control operation of a power supply.

1 7. The integrated circuit of claim 6, wherein said power supply is operable to control
2 operation of a voltage controlled oscillator in said phase-locked loop.

1 8. The integrated circuit of claim 1, wherein said individual circuit is a delay-locked
2 loop.

1 9. The integrated circuit of claim 8, wherein the compensation circuit comprises:
2 a dummy delay line operable to generate a dummy delay line clock signal;
3 a reference source operable to generate a reference clock signal; and
4 a comparator operable to compare the dummy delay line clock signal and the
5 reference clock signal and to generate a control signal therefrom.

1 10. The integrated circuit of claim 9, further comprising a power supply controller
2 operable to control operation of the delay line of said delay-locked loop in response to said
3 control signal.

1 11. The integrated circuit of claim 10, wherein said power supply controller controls
2 operation of said delay line by generating a digital power supply control word (VDD_DLL).

1 12. A method for controlling operation of an integrated circuit, comprising:
2 detecting performance variations of an individual circuit in said integrated circuit,
3 said performance variation being related to aging of said integrated circuit;
4 and
5 generating a compensation signal to change the operating characteristics of said
6 individual circuit to compensate for said performance variation in
7 accordance with an aging-versus time performance curve.

1 13. The method of claim 12, wherein the individual circuit comprises a phase-locked
2 loop.

1 14. The method of claim 13, wherein said compensation signal is generated by a charge
2 pump having multiple legs that can be selectively enabled to change the performance
3 characteristics of said phase-locked loop.

- 1 15. The method of claim 13, wherein compensation signal is generated by a power
- 2 supply controlled by digital control words to selectively change the operating characteristics
- 3 of said phase-locked loop.

- 1 16. The method of claim 13, wherein said compensation signal is generated by a ring
- 2 oscillator operable to approximate the effects of NBTI and to generate a compensation
- 3 signal corresponding thereto.

- 1 17. The method of claim 16, wherein said compensation signal is used to generate
- 2 digital control words to control operation of a power supply.

- 1 18. The method of claim 17, wherein said power supply is operable to control operation
- 2 of a voltage controlled oscillator in said phase-locked loop.

- 1 19. The method of claim 12, wherein said individual circuit is a delay-locked loop.

- 1 20. The method of claim 19, wherein the compensation circuit comprises:
- 2 a dummy delay line operable to generate a dummy delay line clock signal;
- 3 a reference source operable to generate a reference clock signal; and
- 4 a comparator operable to compare the dummy delay line clock signal and the
- 5 reference clock signal and to generate a control signal therefrom.